REMARKS

This application was filed on 2 June 1998 with ten claims, two of which were written in independent form. An amendment broadening the independent claims, Claim 1 and 6, was filed on 4 October 2000 and has been entered. Additional responses to final and non-final rejections were filed on 19 March 2001, 4 September 2001, 18 February 2002, 18 December 2002, 2 June 2003, 11 April 2004, and 12 August 2004 without amending any claims. Appeal Briefs were filed on 3 June 2002, 4 August 2003, and 15 November 2004.

This application has been appealed three times, resulting in great expense and effort by the applicant in addition to the unconscionable delay in receiving the patent rights to which the applicant is entitled. After each appeal, prosecution has been reopened. The Examiner based the most recent re-opening of prosecution on a "new ground of rejection." The applicant respectfully submits the Examiner's rejection of Claims 1-3 and 5-9 under 35 U.S.C. § 102(e) as being anticipated by Yamguchi *et al.* clearly is not a new ground of rejection, but was first raised when prosecution was re-opened for the second time on 13 November 2003.

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,222,515 B1 to Yamaguchi *et al.* ("Yamaguchi"). The applicant respectfully disagrees and submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102.

"A person shall be entitled to a patent unless," creates an initial presumption of patentability in favor of the applicant. 35 U.S.C. § 102. "We think the precise language of 35 U.S.C. § 102 that, "a person shall be entitled to a patent unless," concerning novelty and unobviousness, clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103, see Graham and Adams." *In re Warner*, 379 F.2d 1011, 1016 (C.C.P.A. 1967) (referencing *Graham v. John Deere Co.*, 383 U.S. 1 (1966) and *United States v. Adams*, 383 U.S. 39 (1966)). "As adapted to *ex parte* procedure, *Graham* is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103'." *In re Piasecki*, 745 F.2d 1468 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d at 1016).

"The prima facie case is a procedural tool which, as used in patent examination (as by courts in general), means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the applicant produces no evidence or argument to rebut it." *In re Spada*, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

The applicant respectfully submits the Examiner has failed to meet the burden of proof required to establish a prima facie case of anticipation. Section 2131 of the Manual of Patent Examiner's Procedure provides:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim . . . . *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

With respect to independent Claim 1, the Examiner has failed to provide a prima facie case of anticipation because the Examiner failed to provide any teaching in Yamaguchi of "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 1.

Claim 1 recites "offsetting a first pixel value to form a first offset pixel value" and "offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value."

The Examiner stated, "Yamaguchi et al teaches a system of displaying a digital video data associated with a method comprising: a first pixel value defined by [(3V) is mean effective voltage], see fig. 7B." The Examiner misinterprets Yamaguchi. Yamaguchi does not show,

teach, or even suggest offsetting 3V as suggested by the Examiner. As stated by the Examiner, 3V is the mean effective voltage of the liquid crystal driving source—neither taught by Yamaguchi as a physical voltage available in Yamaguchi nor as a pixel value. As Yamaguchi does not have a 3V pixel value, 3V cannot be offset by a first predetermined amount as required by Claim 1.

The Examiner has failed to read the teachings of the prior art onto the limitations of the claims presented and therefore has failed to establish a prima facie case of anticipation.

The Examiner has failed to point to any teaching in Yamaguchi that the pixel value of digital video data is offset. The Examiner merely points to teachings of Yamaguchi that drive a particular pixel with a two or more voltages in order that the combination of the various voltages will have the same effect as driving the pixel with the average of the various voltages. For example, one embodiment of Yamaguchi drives an LCD element with 4 volts and 2 volts to simulate driving the LCD element with 3 volts.

Thus, rather than showing, teaching, or even suggesting "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 1, Yamaguchi appears to merely teach creating a method of creating additional gray scale levels by sequentially using combinations of voltage levels.

Claim 6 was rejected under 35 U.S.C. § 102(e) as being anticipated by Yamaguchi. The applicant respectfully disagrees and submits the Examiner has failed to present a *prima facie* case of anticipation.

Claim 6 recites, "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value."

The Examiner stated, "Yamaguchi et al teach inherently a logic circuit defined by means for offsetting inherently a first predetermined amount '-1' [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field]."

The Examiner's logic clearly is flawed. Yamaguchi clearly does not have a first 3V pixel value, and therefore Yamaguchi does not inherently teach a logic circuit offsetting the first pixel value as required by the claim.

Claims 2, 3, 5, 7, 8, and 9 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yamaguchi. The applicant respectfully disagrees and submits the Examiner has failed to present a *prima facie* case of anticipation.

Claims 2 and 5 depend from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 1, Yamaguchi does not show, teach, or suggest the limitations of Claim 1, much less the limitations of Claim 1 in combination with the additional limitations of Claims 2 and 5.

Claim 3 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 1, Yamaguchi does not show, teach, or suggest the limitations of Claim 1, much less the limitations of Claim 1 in combination with the additional limitations of Claim 3.

Claim 3 recites, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed."

Claim 8 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 6, Yamaguchi does not show, teach, or suggest the limitations of Claim 6, much less the limitations of Claim 6 in combination with the additional limitations of Claim 7.

Claim 8 recites, "said first offset value is greater than or less than said first pixel value as a function of the spatial location value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value." The Examiner has failed to make a prima facie case of anticipation for this combination of limitations.

The Examiner has failed to make a prima facie case of anticipation for the combination of limitations recited by Claims 3 and 8. The Examiner merely stated, "Yamaguchi et al teach said

first offset pixel value 2V is less than said first pixel value (3V0 as a function of (X-3) of the spatial location ['-1' defined the spatial location] that [(3V) is mean effective voltage] defined to be displayed.

While it is far from clear what the Examiner means by this statement, it clearly falls short of the standard require by *Richardson* referenced above, that the prior art must show "The identical invention must be shown in as complete detail as contained in the . . . claim." The Examiner's rejection of Claims 3 and 8 is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claims 7 and 10 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claim 6, Yamaguchi does not show, teach, or suggest the limitations of Claim 6, much less the limitations of Claim 6 in combination with the additional limitations of Claims 7 and 10.

Claims 4 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi in view of U.S. Patent No. 5,731,802 to Aras *et al.* ("Aras"). The applicant respectfully disagrees and submits the Examiner has failed to establish a *prima facie* case of obviousness.

Claims 4 and 9 depend from Claims 1 and 6, and should be deemed allowable for that reason and on its own merits. For the reasons argued above with respect to Claims 1 and 6, Yamaguchi in view of Aras does not show, teach, or suggest the limitations of Claims 1 and 6, much less the limitations of Claims 1 and 6 in combination with the additional limitations of Claims 4 and 9.

Claim 4 recites, "wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." Claim 9 recites, "wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame."

The Examiner has not read the teachings of Yamaguchi and Aras onto the recited limitations of the claims, but instead seems to be claiming some inherent relationship between data transitions and bit transitions of the bit-planes.

In view of the amendments and the remarks presented herewith, it is believed that the claims currently in the application accord with the requirements of 35 U.S.C. § 112 and are allowable over the prior art of record. Therefore, it is urged that the pending claims are in condition for allowance. Reconsideration of the present application is respectfully requested.

Respectfully submitted,

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